EVALUATION OF AN ULTRA-LOW POWER REED SOLOMON ENCODER FOR NASA'S SPACE TECHNOLOGY 5 MISSION

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Abstract

Radiation test results and analyses are presented for ultra-low power Reed Solomon encoder circuits that are being considered for use on the Space Technology 5 (ST5) mission. The total ionizing dose tolerance is in excess of 100 krad(Si) and is due to the low supply voltage and the use of back-bias, which suppresses radiation-induced leakage currents in the n-channel devices. The circuits do not latch-up for ion LET values of at least 60 MeV-cm^2/mg. A hardened-by-design approach to SEU has achieved an upset threshold of about 18 MeV-cm^2/mg. The SEU rate expected for these circuits in the geosynchronous transfer orbit of ST5 is low.

Introduction

Two important issues that must be dealt with during spacecraft subsystem design are the power consumption and radiation tolerance of microelectronic components. Over the last decade an approach to these problems for active CMOS circuits has evolved that is distinct from traditional approaches. The low power aspect of the approach originated with Stanford's Ultra Low Power (ULP) CMOS Project [1]. This recognizes that CMOS circuits with high activity levels do not require low DC power dissipation. Thus, unlike standard CMOS circuits, which strive for low DC leakage currents, the ULP approach is based on balancing the AC (switching) and DC power dissipation so that they both account for about 50% of the power loss. This is accomplished by aggressively scaling the supply voltage (V_{dd}) and the transistor threshold voltage (V_t). Illustrative results for this are shown in Figure 1. This shows the power consumed in a 1 million transistor design as V_{dd} and V_t are scaled so that the circuit maintains a constant performance or speed. A 10% circuit activity is assumed. In addition, transistors are assumed to have a 1 μA on current and a subthreshold slope of 80 mV/decade. Shown along the abscissa are the V_{dd} values and the corresponding V_t values. The result on the far left is typical of 3.3 V CMOS technology. The transistors have V_t = 660 mV and the power dissipation is almost entirely AC. In principle, scaling these two parameters down together allows the circuit's performance to remain constant, while the power reduction is dramatic. The AC and DC power dissipation become approximately equal at V_{dd} = 0.5 V and V_t = 100 mV, which are typical of ULP circuits.

The native n-channel and p-channel transistor thresholds for the ULP process are set to very near zero and back-bias voltage control on the substrate and well are utilized to electrically control the effective thresholds. The optimum back-bias voltage levels where AC and DC power are balanced for any specific application is a function of required application speed as well as chip design architecture and data activity. The back-bias levels can be selected to effectively trade excess chip speed capability not required for a particular application in return for reduced total power. Higher native threshold n-channel and p-channel transistors can also be provided for use in low activity sections of a design. In the future, the use of ULP in a twin-well process could provide capability to apply multiple bias levels and resulting effective thresholds within different sections of the chip.

This technology was geared more toward space applications and further developed at the University of Idaho, Center for Advanced Microelectronic and Biomolecular Research (CAMBR) [2,3], where single event upset mitigation design was introduced [4]. It became known as **C**MOS **U**ltra-**L**ow **P**ower **R**adiation **T**olerant (**CULPR**i**T**) in a Department of Defense sponsored program, in which it was demonstrated that the technology is total dose tolerant at the transistor level [5]. This made a more realistic case in favor of using it for space applications because it then became unnecessary to modify the processing to achieve total dose hardened circuits.

The decision was subsequently made to use CULPRiT Reed Solomon (RS) Encoders on NASA's ST5 mission. This mission is a part of the New Millenium Program, which attempts to validate breakthrough technologies and infuse them into future missions. Reduction of satellite size, weight and cost is also a primary objective. ST5 will consist of 3 nanosats, each weighing about 47 pounds. They will be put into a geosynchronous transfer orbit (GTO) for a 3 month mission. The CULPRiT RS Encoder design contains 164,000 transistors and is functionally equivalent to another RS Encoder previously designed by CAMBR utilizing Aeroflex/UTMC radiation hardened technology and meets the requirements of the Consultative Committee for Space Data Systems (CCSDS) telemetry channel coding, which has a broad space heritage [6,7]. This paper reports on radiation tests, analysis and prediction of the performance of the CULPRiT RS Encoders for the ST5 mission.

Hardness By Design

The Single Event Upset (SEU) tolerant Whitaker cell, shown in Figure 2 with access and buffer transistors omitted for simplicity, has proven to be very successful and has been utilized both in full custom microcircuits for space applications [8] and as the memory cell basis for a radiation tolerant standard cell library [9]. However, the reduced voltage swing at cell interior storage nodes due to p-channel pull down transistors M3 and M4 at Y0 and Y1 and n-channel pull up transistors M9 and M10 at Y2 and Y3 became problematic to the performance of the cell at the aggressively scaled CULPRiT operating voltage.

A formal design synthesis and analysis technique based on the theory of asynchronous sequential circuits has been developed at CAMBR and used to create a new Single Event Resistant Topology (SERT) cell design utilized for the CULPRiT RS Encoder design [10]. The SERT cell, shown in Figure 3, again with access and buffer transistors omitted for simplicity, utilizes fully complementary p-channel pull-ups and n-channel pull-downs for all nodes. Unlike the Whitaker design, the SERT cell is conflict free during SEU recovery. That is, when a particle strike causes an upset of one storage node the SERT cell feedback is designed to allow nodes to enter a high impedance or tri-state mode, but in no case will one of the storage nodes be pulled up and be pulled down simultaneously. This design feature decreases the power consumption of the cell during SEU recovery and also means that the SEU recovery is never dependent on the relative strength of transistors. This makes the transistor sizing effort much less critical to SEU immunity.

Results

Power Consumption

For comparison purposes, the new Encoder design was implemented both in the AMI Semiconductor (AMIS) 3.3 V, 0.35 μm (C3) bulk CMOS process as well as the 0.5

V ULP bulk CMOS process. The ULP process utilizes the same fabrication equipment and similar flows but does require additional processing steps compared to the standard CMOS. Measurements of the Encoder core power only, excluding the power required to drive the I/O pads and related board capacitance at a data rate of 80Mbp (10MHz clock) indicate a core CULPRiT power savings factor of nearly 70X compared to the C3 process. The core power of the CULPRiT Encoder was measured to be 1.0 mW @ 10MHz while a C3 Encoder core power was 68 mW @ 10MHz. The CULPRiT encoder was created in two versions, one interfacing external to the chip at 0.5V signal levels and one including on-chip level shifters which interface externally at 3.3V. When measured on an HP 82000 IC tester whose coaxial leads and data comparators present a load of approximately 120pf to the unit under test the I/O power required to drive 3.3V Encoder I/O signals at 10 MHz is approximately 70 mW. Considering the potential core power savings vs. I/O power requirements highlights the value of complete CULPRiT systems or subsystems over discrete CULPRiT components as well as highlighting the applicability of low power signaling schemes such a Low Voltage Differential Signaling (LVDS). By further comparison, the typical power consumption of the Aeroflex/UTMC radiation hard technology version RS Encoder flying in many spacecraft today is 350 mW (driving 50pf loads at 10MHz). By offering orders of magnitude savings in power consumption CULPRiT is a potentially enabling technology for nanosats.

Total Ionizing Dose

It has been shown previously why CULPRiT technology is much more total dose tolerant than the corresponding standard commercial CMOS technology at the device level [5]. Standard CMOS technology typically fails due to radiation-induced leakage currents in the field oxide region. First, the reduced gate bias used for CULPRiT limits the yield of radiation-induced holes in the field oxide. Second, the back-gate (substrate) bias used to control the low threshold voltages in CULPRiT technology increases the threshold voltage of the n-channel field oxide, thus suppressing radiation-induced parasitic currents. This effect is shown in Figure 4, where it can be seen that the application of a rather small back-bias suppresses substantial leakage current. Total dose testing at the device level showed that the AMIS standard CMOS process was tolerant to about 30 krad(Si), while the corresponding AMIS CULPRiT technology was tolerant to over 200 krad(Si).

This level of total dose tolerance is expected to carry over to the circuit performance. The RS Encoders were tested at the NASA/GSFC Co-60 gamma ray facility under static bias conditions according to Mil-Standard 1019.5. The back-bias applied during the test was chosen to optimize encoder performance at V_{dd} = 0.5 V. This turned out to be a p-channel back-bias of 2.0 V and an n-channel back-bias of –1.4 V. No degradation of performance in terms of leakage current, timing or functionality was observed at doses up to 100 krad(Si). The ST5 mission is 3 months in duration so this test is more than sufficient to qualify the encoder from a total dose perspective.

Single Event Effects

Heavy ion tests were done at the Brookhaven National Laboratory tandem Van de Graaff accelerator. The encoders were exercised during the test. Various combinations of supply voltages and back-biases were used with the idea that it may be possible to trade circuit performance for increased SEE resistance. Supply voltages ranged from 0.5 to 0.8 V while the magnitude of the back-biases ranged from 1.4 to 2.5 V.

There was no latch-up observed out to effective LET values of 60 MeV-cm^2/mg. This was expected mainly because of the low supply voltages. The SEU cross section as a function of effective LET is shown in Figure 5. All the data shown in this Figure is for V_{dd} = 0.5 V, which is the supply voltage that is planned to be used on the ST5 mission. The values of back-bias are those discussed above to allow for optimal performance at a supply voltage of 0.5 V. When different combinations of p-channel and n-channel back-biases were used, it was observed that the change of back-bias in the range considered here had minimal effect.

The SEU results in Figure 5 show an ion or angle dependent effect that is not understood. Thus, a worst-case Weibull fit was made to the data as shown by the solid line in the Figure. According to this fit, the LET threshold for SEU is about 18 MeV-cm^2/mg. Thus, the encoders will not experience proton-induced SEU. The saturation cross section is about 17 μm^2/bit, indicating a low SEU rate. This was used with the CREME96 suite of programs [11] to calculate SEU rates for the ST5 mission. Calculations were done for an elliptical orbit with a 200 km perigee, 35,790 km apogee and 0 degree inclination. The shielding level was assumed to be 100 mils of aluminum.

The SEU rates due to galactic cosmic rays (GCR) during solar minimum and solar maximum were calculated. In addition, the rates for a worst-case solar particle event (SPE) during the peak 5 minutes, worst day and worst week were also obtained. CREME96 assumes the well-known October 1989 event is the basis for these results, shown in the table below. It is seen that these projected rates for the ST5 mission are low.

SEU Rates for 2048 bit CULPRiT RS Encoders Expected During the ST5 Mission

Condition:	#SEU/(bit-day):
GCR (solar minimum)	7.50E-9
GCR (solar maximum)	9.20E-10
Worst Case SPE (peak 5 minutes)	3.30E-5
Worst Case SPE (worst day)	9.20E-6
Worst Case SPE (worst week)	2.70E-6

Conclusions

CULPRiT RS Encoders have been tested and analyzed for suitability on the ST5 mission. The total ionizing dose tolerance of the circuits is in excess of 100 krad(Si), consistent with previous testing at the device level. The hardness by design approach to SEU mitigation has resulted in an upset threshold of about 18 MeV-cm^2/mg. Thus, it appears to be reasonable to fly the circuits on the relatively short duration ST5 mission.

References

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Figures

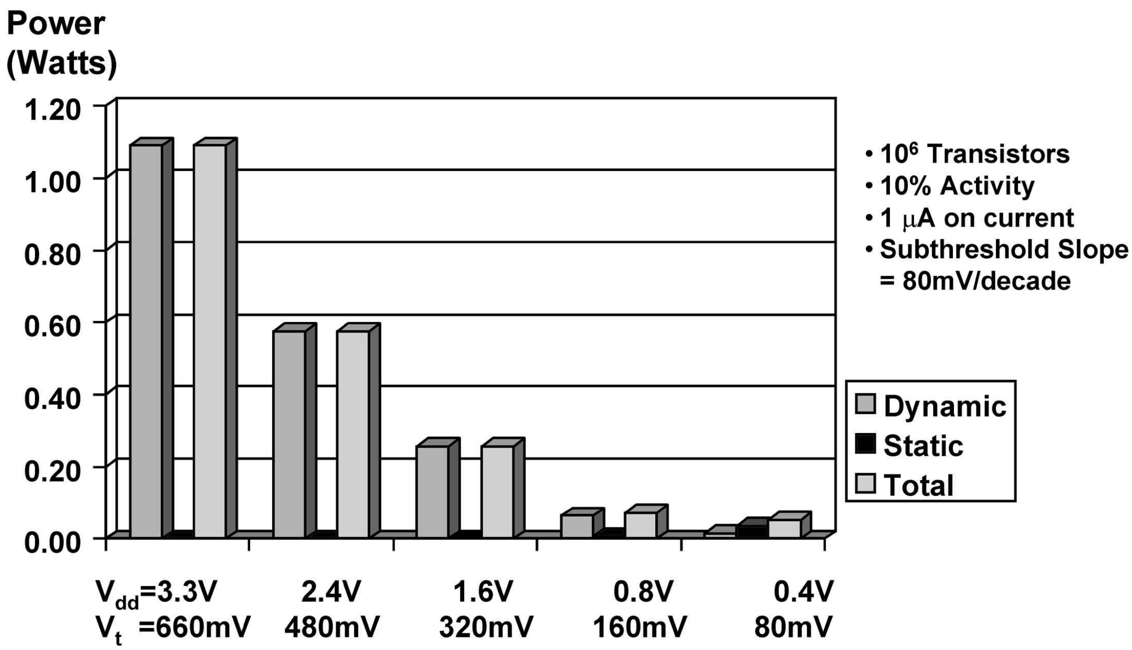

Fig. 1. Power consumption scaling at constant circuit performance.

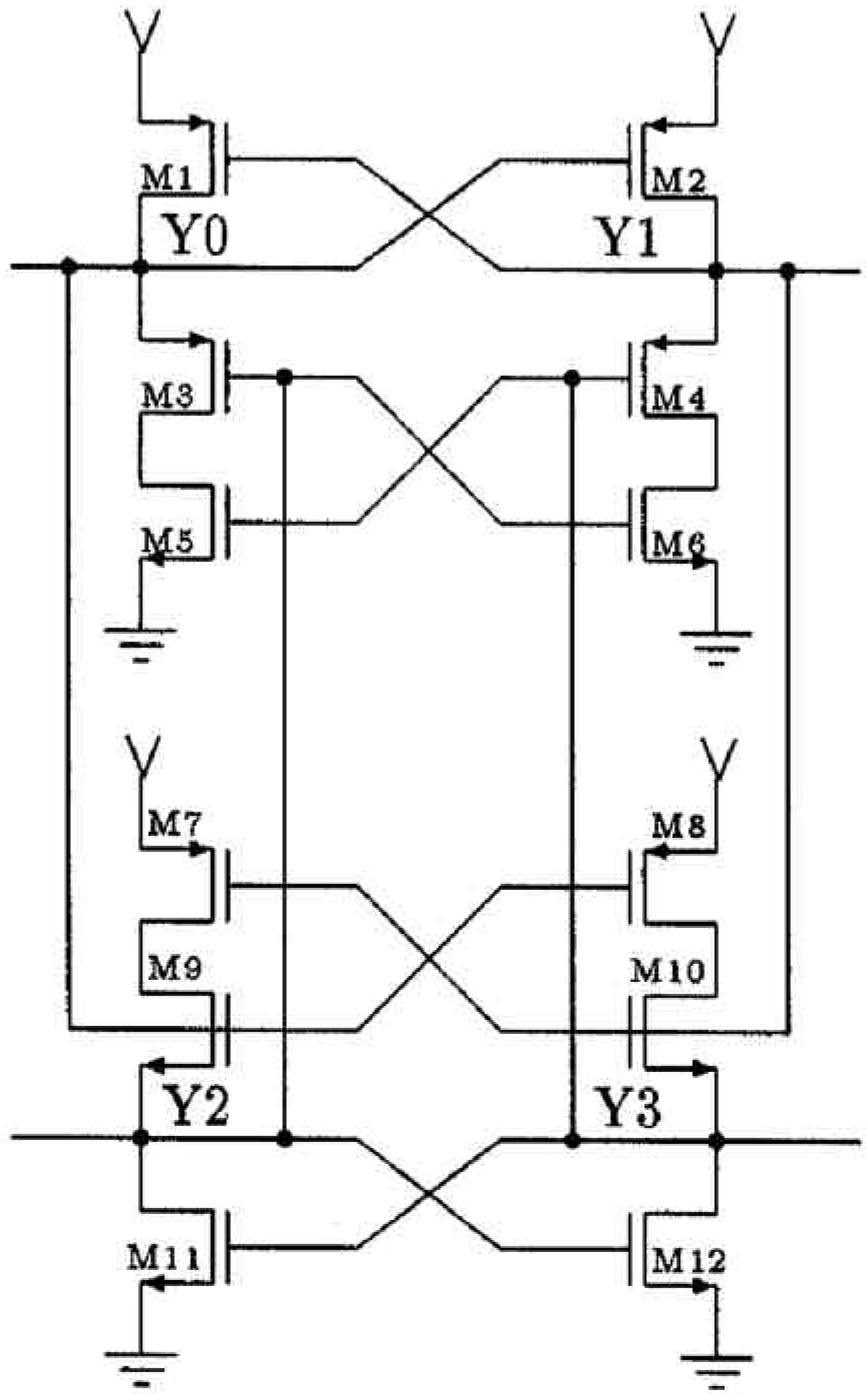

Fig.2. Whitaker SEU Tolerant Cell.

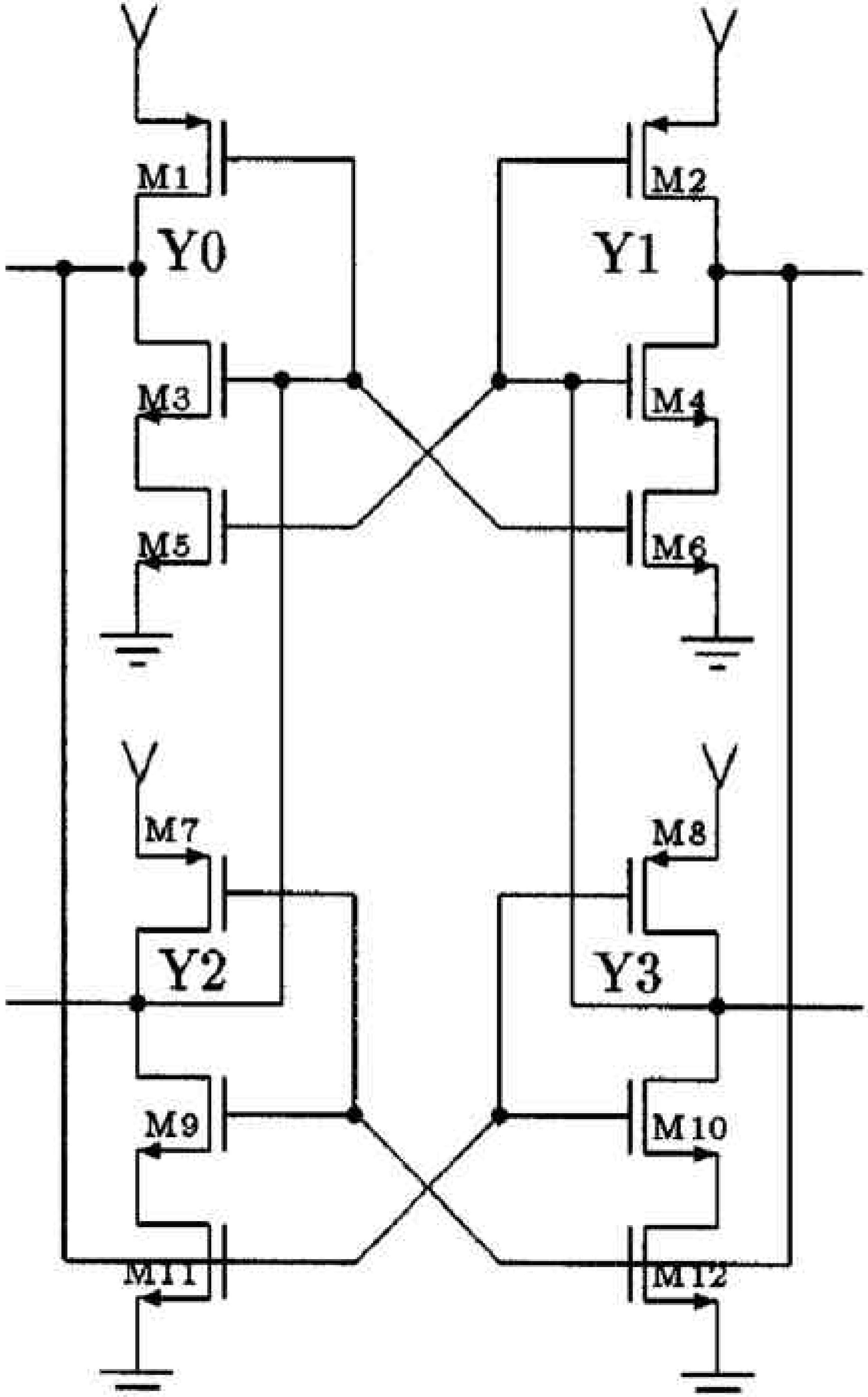

Fig.3. SERT SEU Tolerant Cell.

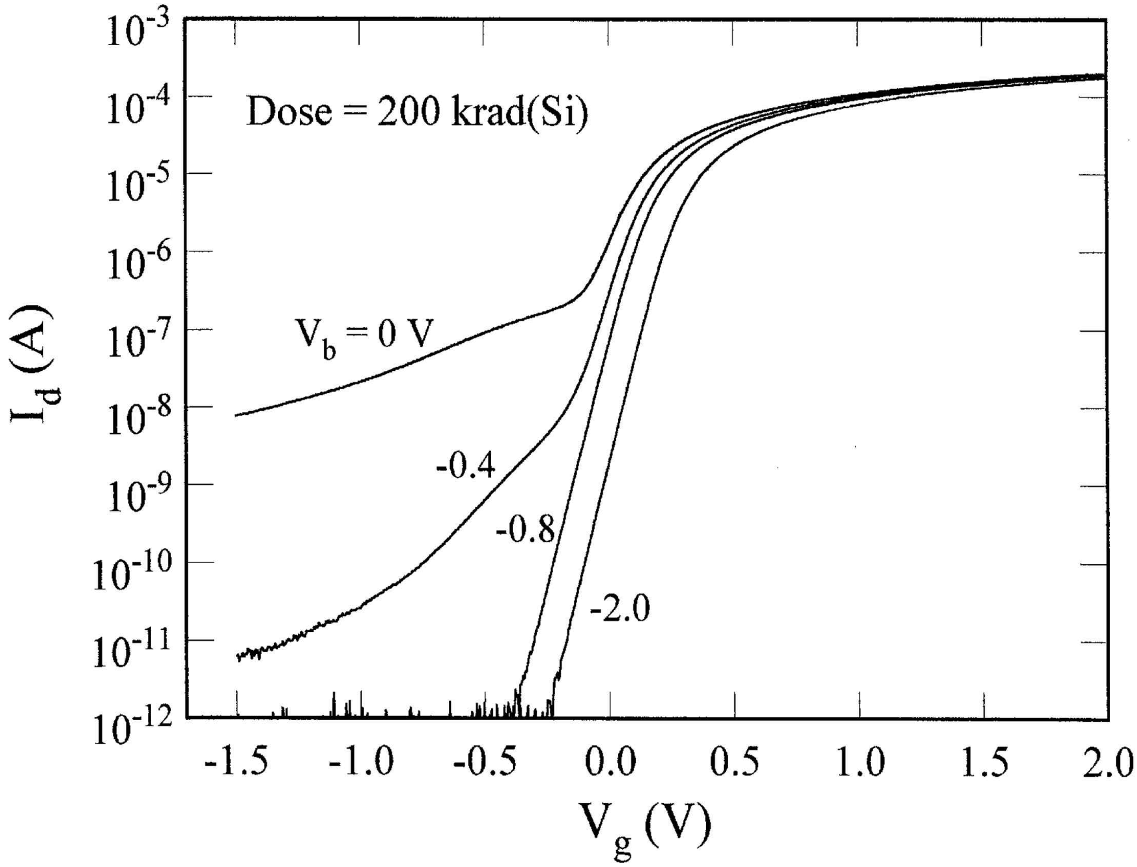

Fig.4. Effect of back-bias on CULPRiT n-channel transistors (from ref. 5).

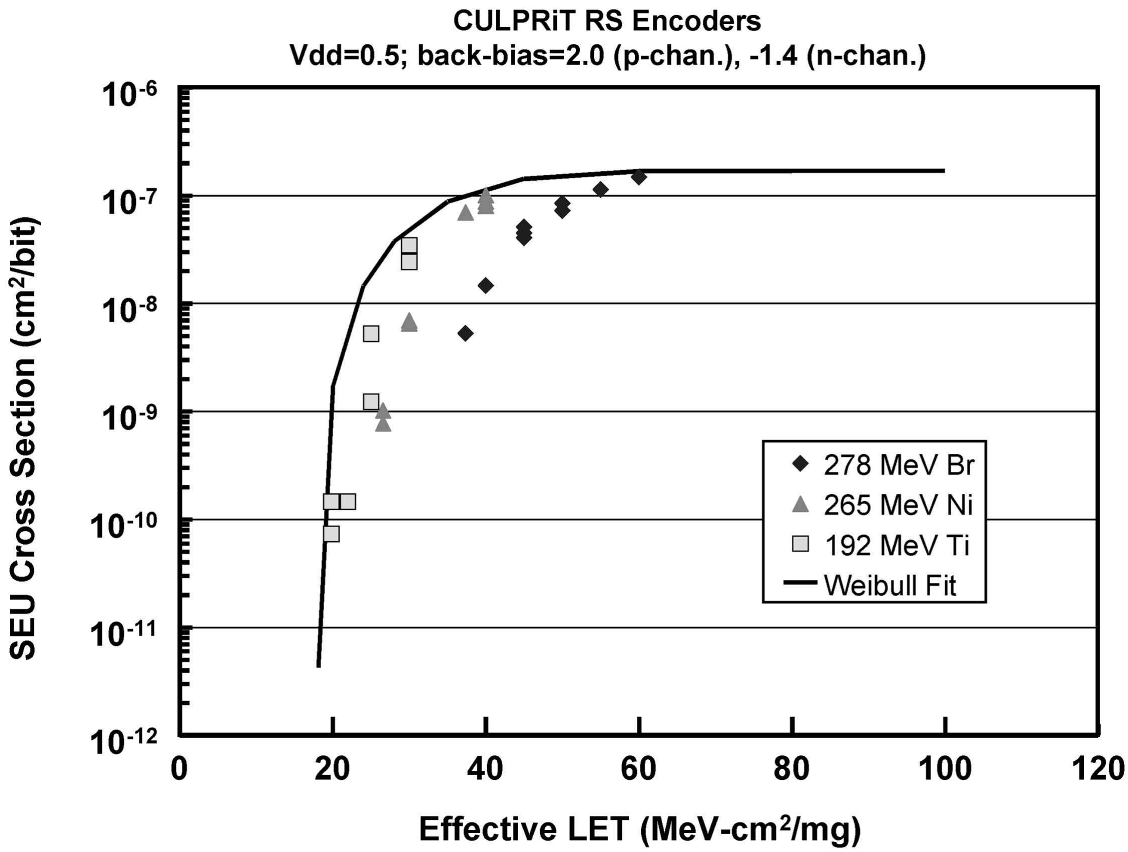

Fig. 5. Heavy ion SEU cross sections of CULPRiT RS Encoders as a function of LET.